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Substitute for form 1449A/PTO

Complete if Known

Application Number	10/667,871
Filing Date	September 22, 2003
First Named Inventor	Yeo, et al.
Art Unit	2811
Examiner Name	Unknown

Sheet

1

of

2

Attorney Docket Number

TSM03-0553

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code ² (if known)			
SM	A	US-4,314,269	02-02-1982	Fujiiki	
SM	B	US-5,629,544	05-13-1997	Voldman, et al.	
SM	C	US-5,811,857	09-22-1998	Assaderagh, et al.	
SM	D	US-6,008,095	12-28-1999	Gardner, et al.	
SM	E	US-6,015,893	01-18-2000	Voldman, et al.	
SM	F	US-6,232,163 B1	05-15-2001	Voldman, et al.	
SM	G	US-6,258,664 B1	07-10-2001	Reinberg	
SM	H	US-6,294,834 B1	09-25-2001	Yeh, et al.	
SM	I	US-6,358,791 B1	03-19-2002	Hsu, et al.	
SM	J	US-2002/0153549 A1	10-24-2002	Laibowitz, et al.	
SK	K	US-6,475,838 B1	11-05-2002	Bryant, et al.	
SK	L	US-6,489,664 B2	12-03-2002	Re, et al.	
SK	M	US-2003/0030091 A1	02-13-2003	Bulsara, et al.	
SM	N	US-6,524,905 B2	02-25-2003	Yamamichi, et al.	
SM	O	US-2003/0080386 A1	05-01-2003	Ker, et al.	
SM	P	US-6,558,998 B2	05-06-2003	Belleville, et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Country Code ³ - Number ⁴ - Kind Code ⁵ (if known)				
SM	Q	WO 03/017336 A2	02-27-2003	Amberwave Systems Corporation		

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
SM	R	WANG, L.K., et al., "On-Chip Decoupling Capacitor Design to Reduce Switching-Noise-Induced Instability in CMOS/SOI VLSI," Proceedings of the 1995 IEEE International SOI Conference, Oct. 1995, pp.100-101.	
SM	S	YEOH, J.C., et al., "MOS Gated Si:SiGe Quantum Wells Formed by Anodic Oxidation," Semicond. Sci. Technol. (1998), Vol. 13, pp. 1442-1445, IOP Publishing Ltd., UK.	
SM	T	CAVASSILAS, N., et al., "Capacitance-Voltage Characteristics of Metal-Oxide-Strained Semiconductor Si/SiGe Heterostructures," Nanotech 2002, Vol. 1, pp. 600-603.	

Examiner Signature		Date Considered	March 2, 2005
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Substitute for form 1449B/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(use as many sheets as necessary)

(use as many sheets as necessary)

Sheet

2

of

2

Complete if Known

Application Number	10/667,871
Filing Date	September 22, 2003
First Named Inventor	Yeo, <i>et al.</i>
Group Art Unit	2811
Examiner Name	Unknown
Attorney Docket Number	TSM03-0553

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Signature	<i>June M. Kennedy</i>	Date Considered	
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				Application Number	10/667,871
Sheet	2	of	3	Filing Date	September 22, 2003
				First Named Inventor	Yeo, et al.
				Group Art Unit	2811
				Examiner Name	TBD
				Attorney Docket Number	TSM03-0553

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Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.				T ²
QH	23	ISMAIL, K., et al., "Electron Transport Properties of Si/SiGe Heterostructures: Measurements and Device Implications," Applied Physics Letters, Vol. 63, No. 5, (August 2, 1993), pp. 660-662.				
QH	24	NAYAK, D.K., et al., "Enhancement-Mode Quantum-Well Ge _x Si _{1-x} PMOS," IEEE Electron Device Letters, Vol. 12, No. 4, (April 1991), pp. 154-156.				
JH	25	GÁMIZ, F., et al., "Strained-Si/SiGe-on-Insulator Inversion Layers: The Role of Strained-Si Layer Thickness on Electron Mobility," Applied Physics Letters, Vol. 80, No. 22, (June 3, 2002), pp. 4160-4162.				
JH	26	GÁMIZ, F., et al., "Electron Transport in Strained Si Inversion Layers Grown on SiGe-on-Insulator Substrates," Journal of Applied Physics, Vol. 92, No. 1, (July 1, 2002), pp. 288-295.				
QH	27	MIZUNO, T., et al., "Novel SOI p-Channel MOSFETs With Higher Strain in Si Channel Using Double SiGe Heterostructures," IEEE Transactions on Electron Devices, Vol. 49, No. 1, (January 2002), pp. 7-14.				
JH	28	TEZUKA, T., et al., "High-Performance Strained Si-on-Insulator MOSFETs by Novel Fabrication Processes Utilizing Ge-Condensation Technique," Symposium On VLSI Technology Digest of Technical Papers, (2002), pp. 96-97.				
QH	29	JURCZAK, M., et al., "Silicon-on-Nothing (SON) – an Innovative Process for Advanced CMOS," IEEE Transactions on Electron Devices, Vol. 47, No. 11, (November 2000), pp. 2179-2187.				
QH	30	JURCZAK, M., et al., "SON (Silicon on Nothing) – A NEW DEVICE ARCHITECTURE FOR THE ULSI ERA," Symposium on VLSI Technology Digest of Technical Papers, (1999), pp. 29-30.				
QH	31	MAITI, C.K., et al., "Film Growth and Material Parameters," Application of Silicon-Germanium Heterostructure, Institute of Physics Publishing, Ch. 2 (2001) pp. 32-42.				
QH	32	TIWARI, S., et al., "Hole Mobility Improvement in Silicon-on-Insulator and Bulk Silicon Transistors Using Local Strain," International Electron Device Meeting, (1997), pp. 939-941.				
QH	33	OOTSUKA, F., et al., "A Highly Dense, High-Performance 130nm Node CMOS Technology for Large Scale System-on-a-Chip Applications," International Electron Device Meeting, (2000), pp. 575-578.				
QH	34	MATTHEWS, J.W., et al., "Defects in Epitaxial Multilayers – I. Misfit Dislocations," Journal of Crystal Growth, Vol. 27, (1974), pp. 118-125.				
QH	35	MATTHEWS, J.W., et al., "Defects in Epitaxial Multilayers – II. Dislocation Pile-Ups, Threading Dislocations, Slip Lines and Cracks," Journal of Crystal Growth, Vol. 29, (1975), pp. 273-280.				

Examiner Signature	<i>Paul M. Kennedy</i>	Date Considered	<i>March 2, 2005</i>
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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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Substitute for form 1449B/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)				Application Number	10/667,871
Sheet	3	of	3	Filing Date	September 22, 2003
				First Named Inventor	Yeo, et al.
				Group Art Unit	2811
				Examiner Name	TBD
				Attorney Docket Number	TSM03-0553

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS				
Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.		T ²
JK	36	MATTHEWS, J.W., et al., "Defects in Epitaxial Multilayers – III. Preparation of Almost Perfect Multilayers," Journal of Crystal Growth, Vol. 32, (1976), pp. 265-273.		
JK	37	SCHÖPPEN, A., et al., "Mesa and Planar SiGe-HBTs on MBE-Wafers," Journal of Materials Science: Materials in Electronics, Vol. 6, (1995), pp. 298-305.		
JK	38	MATTHEWS, J.W., "Defects Associated with the Accommodation of Misfit Between Crystals," J. Vac. Sci. Technol., Vol. 12, No. 1 (Jan./Feb. 1975), pp. 126-133.		
JK	39	HUANG, X., et al., "Sub-50 nm P-Channel FinFET," IEEE Transactions on Electron Devices, Vol. 48, No. 5, May 2001, pp. 880-886.		
JK	40	SHAHIDI, G.G., "SOI Technology for the GHz Era," IBM J. Res. & Dev., Vol. 46, No. 2/3, March/May 2002, pp. 121-131.		
JK	41	SHIMIZU, A., et al., "Local Mechanical Stress Control (LMC): A New Technique for CMOS-Performance Enhancement," IEDM 2001, pp. 433-436.		
JK	42	WONG, H.-S.P., "Beyond the Conventional Transistor," IBM J. Res. & Dev., Vol. 46, No. 2/3, March/May 2002, pp. 133-167.		
JK	43	YANG, F.L., et al., "25 nm CMOS Omega FETs," IEDM 2002, pp. 255-258.		
JK	44	YANG, F.L., et al., "35nm CMOS FinFETs," 2002 Symposium on VLSI Technology Digest of Technical Papers, 2002, pp. 104-105.		
JK	45	THOMPSON, S., et al., "A 90 nm Logic Technology Featuring 50nm Strained Silicon Channel Transistors, 7 Layers of Cu Interconnects, Low k ILD, and 1 um ² SRAM Cell," IEDM, pp. 61-64.		
JK	46	WELSER, J., et al., "NMOS and PMOS Transistors Fabricated in Strained Silicon/Relaxed Silicon-Germanium Structures," IEDM 1992, pp. 1000-1002.		
Examiner Signature	<i>Janet Kennedy</i>		Date Considered	March 2, 2005

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<p>Substitute for form 1449/PTO</p> <p>INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i></p>				<p>Complete if Known</p> <table border="1"> <tr> <td>Application Number</td> <td>10/667,871</td> </tr> <tr> <td>Filing Date</td> <td>September 22, 2003</td> </tr> <tr> <td>First Named Inventor</td> <td>Yeo, et al.</td> </tr> <tr> <td>Art Unit</td> <td>2811</td> </tr> <tr> <td>Examiner Name</td> <td>TBD</td> </tr> <tr> <td>Attorney Docket Number</td> <td>TSM03-0553</td> </tr> </table>		Application Number	10/667,871	Filing Date	September 22, 2003	First Named Inventor	Yeo, et al.	Art Unit	2811	Examiner Name	TBD	Attorney Docket Number	TSM03-0553
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Sheet	1	of	1														

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